I CLAIM:

1. A phase-locked loop system configured to cause an output signal to tend toward a desired output frequency, the desired output frequency being a factor of a reference frequency associated with an applied reference signal, comprising:

a charge pump system configured to produce a charge pump output based on differences detected between the output signal and the desired output frequency; and

an oscillator operatively coupled with the charge pump system and configured to produce the output signal based on the charge pump output,

where the charge pump system is configured to selectively effect proportional control over the output signal by applying a correcting pulse along a proportional control path of the phase-locked loop system,

and where the charge pump system includes a correction circuit configured to receive the correcting pulse and produce a plurality of smaller correcting pulses to reduce jitter in the output signal.

2. The phase-locked loop system of claim 1, where the correcting circuit includes a sampling capacitance and an output capacitance, the correcting circuit being configured so that the sampling capacitance accumulates a charge corresponding to the correcting pulse and then repeatedly dumps such charge to the output capacitance to produce the smaller correcting pulses.

3. The phase-locked loop system of claim 2, where the correcting circuit is configured so that periodic dumping of the charge on the sampling capacitance is timed with cycles of the output signal.

4. The phase-locked loop system of claim 2, where the sampling capacitance is repeatedly reset according to a timing determined by cycles of the reference signal.

5. The phase-locked loop system of claim 2, where the sampling capacitance and output capacitance are scaled relative to one another according to a frequency relationship between the reference signal and the output signal.

6. The phase-locked loop system of claim 5, where the sampling capacitance is x/y times greater than the output capacitance, where x/y is the factor by which the phase-locked loop system is configured to multiply the reference frequency to produce the desired output frequency.

7. The phase-locked loop system of claim 2, where the sampling capacitance and output capacitance are configured so that the correction circuit outputs substantially as much charge as it receives.

8. The phase-locked loop system of claim 1, where the correcting circuit is configured to produce a smaller correcting pulse for each cycle of the output signal.

9. The phase-locked loop system of claim 1, where the charge pump system includes an individual charge pump configured to provide both integrating and proportional control over the output signal via operation of a switched filter network, where the switched filter network is coupled to the charge pump within the proportional control path and within an integrating control path of the phase-locked loop system.

10. A phase-locked loop system configured to cause an output signal to tend toward a desired output frequency, the desired output frequency being a factor of a reference frequency associated with an applied reference signal, comprising:

a charge pump system configured to produce a charge pump output based on differences detected between the output signal and the desired output frequency; and

an oscillator operatively coupled with the charge pump system and configured to produce the output signal based on the charge pump output,

where the charge pump system is configured to selectively effect proportional control over the output signal by producing a correcting pulse having a duration, and applying the correcting pulse to a proportional control path of the phase-locked loop system,

and where the charge pump system includes a correction circuit configured to receive the correcting pulse and convert the correcting current pulse into a charge-equivalent current that is output over a period of time that is greater than the duration of the correcting pulse.

11. The phase-locked loop system of claim 10, where the charge pump system includes an individual charge pump configured to provide both integrating and proportional control over the output signal via operation of a switched filter network, where the switched filter network is coupled to the charge pump within the proportional control path and within an integrating control path of the phase-locked loop system.

12. The phase-locked loop system of claim 10, where the charge-equivalent current is substantially constant during a plurality of cycles of the output signal.

13. The phase-locked loop system of claim 12, where the charge-equivalent current is substantially constant during a number of cycles of the output signal that substantially corresponds in duration to one cycle of the reference signal.

14. The phase-locked loop system of claim 10, where the correction circuit includes a sampling capacitance configured to store a charge corresponding to the correcting pulse, and where such charge is applied to a voltage controlled current source to produce the charge-equivalent current.

15. The phase-locked loop system of claim 14, where the voltage controlled current source has an associated gain value, the associated gain value being selected based on a ratio of the reference frequency to the desired output frequency.

16. The phase-locked loop system of claim 10, where the correction circuit is one of a plurality of correction circuits with staggered duty cycles, the correction circuits being configured so that one of the correction circuits produces a charge-equivalent current corresponding to a first correcting pulse while another correction circuit resets and waits for a second correcting pulse.

17. The phase-locked loop system of claim 10, where the correction circuit is part of a switched filter network configured to provide both integrating and proportional control over the output signal.

18. The phase-locked loop system of claim 17, where the correction circuit includes a sampling capacitance configured to receive the correcting pulse and store a charge corresponding to the correcting pulse, the switched filter network being configured to first apply such charge to a proportional control path of the phase-locked loop system, and then apply at least a portion of such charge to an integrating control path of the phase-locked loop system.

19. A phase-locked loop system configured to cause an output signal to tend toward a desired output frequency, the desired output frequency being a factor of a reference frequency associated with an applied reference signal, comprising:

a charge pump system configured to produce a charge pump output based on differences detected between the output signal and the desired output frequency; and

an oscillator operatively coupled with the charge pump system and configured to produce the output signal based on the charge pump output,

where the charge pump system is configured to selectively effect proportional control over the output signal by producing a correcting pulse having a duration and applying the correcting pulse to a proportional control path of the phase-locked loop system,

and where the charge pump system includes a correcting circuit having a sampling capacitance configured to receive the correcting pulse and store a corresponding correcting charge, the correcting circuit being configured to output the correcting charge over a period of time that is greater than the duration of the correcting pulse.

20. The phase-locked loop system of claim 19, where the correcting circuit further includes an output capacitance, the correcting circuit being configured so that the sampling capacitance repeatedly dumps the correcting charge to the output capacitance to produce a plurality of smaller correcting pulses corresponding to the correcting pulse.

21. The phase-locked loop system of claim 20, where the correcting circuit is configured so that periodic dumping of the charge on the sampling capacitance is timed with cycles of the output signal.

22. The phase-locked loop system of claim 20, where the sampling capacitance is repeatedly reset according to a timing determined by cycles of the reference signal.

23. The phase-locked loop system of claim 20, where the sampling capacitance and output capacitance are scaled relative to one another according to a frequency relationship between the reference signal and the output signal.

24. The phase-locked loop system of claim 23, where the sampling capacitance is x/y times greater than the output capacitance, where x/y is the factor by which the phase-locked loop system is configured to multiply the reference frequency to produce the desired output frequency.

25. The phase-locked loop system of claim 20, where the sampling capacitance and output capacitance are configured so that the correction circuit outputs substantially as much charge as it receives.

26. The phase-locked loop system of claim 20, where the correcting circuit is configured to produce a smaller correcting pulse for each cycle of the output signal.

27. The phase-locked loop system of claim 19, where the charge pump system includes an individual charge pump configured to provide both integrating and proportional control over the output signal via operation of a switched filter network associated with the correction circuit, where the switched filter network is coupled to the charge pump within the proportional control path and within an integrating control path of the phase-locked loop system.

28. The phase-locked loop system of claim 19, where the correction circuit is configured to output a charge-equivalent current based on the correcting pulse and corresponding correcting charge.

29. The phase-locked loop system of claim 28, where the charge-equivalent current is substantially constant during a plurality of cycles of the output signal.

30. The phase-locked loop system of claim 29, where the charge-equivalent current is substantially constant during a number of cycles of the output signal that substantially corresponds in duration to one cycle of the reference signal.

31. The phase-locked loop system of claim 28, where the correction circuit is configured to apply the correcting charge to a voltage controlled current source to produce the charge-equivalent current.

32. The phase-locked loop system of claim 31, where the voltage controlled current source has an associated gain value, the associated gain value being selected based on a ratio of the reference frequency to the desired output frequency.

33. The phase-locked loop system of claim 28, where the correction circuit is one of a plurality of correction circuits with staggered duty cycles, the correction circuits being configured so that one of the correction circuits produces a charge-equivalent current corresponding to a first correcting pulse while another correction circuit resets and waits for a second correcting pulse.

34. A method of reducing jitter in a phase-locked loop system configured to produce an output signal having an output frequency which is a factor of a reference frequency associated with an applied reference signal, the method comprising:

receiving a correcting pulse from a charge pump system configured to selectively effect proportional control over the output signal by producing such a correcting pulse and applying the correcting pulse to a proportional control path of the phase-locked loop system, where the received correcting pulse has a duration;

storing a correcting charge based on the correcting pulse at a sampling capacitance; and

outputting the correcting charge to control an oscillator which generates the output signal, where the outputting of the correcting charge occurs over a period of time that is greater than the duration of the correcting pulse.

35. The method of claim 34, further comprising providing integrating and proportional control over the output signal based on output from a single charge pump included with the charge pump system.

36. The method of claim 34, where outputting the correcting charge includes outputting a plurality of smaller correcting pulses corresponding to the received correcting pulse.

37. The method of claim 36, where outputting the correcting charge includes repeatedly dumping charge from the sampling capacitance to an output capacitance to produce the plurality of smaller correcting pulses.

38. The method of claim 36, where the output frequency is N times the reference frequency, and where outputting a plurality of smaller correcting pulses includes outputting N smaller correcting pulses for each received correcting pulse.

39. The method of claim 34, where outputting the correcting charge includes outputting a portion of the correcting charge during each of a plurality of cycles of the output signal.

40. The method of claim 34, where outputting the correcting charge includes outputting a charge-equivalent current corresponding to the correcting pulse.

41. The method of claim 40, where the charge-equivalent current is output over substantially all of one cycle of the reference signal.

42. The method of claim 34, where outputting the correcting charge includes outputting a plurality of smaller correcting pulses corresponding to the correcting pulse, where the smaller correcting pulses are output at a correction frequency that is greater than a receive frequency associated with the correcting pulse.

43. A phase-locked loop configured to produce an output signal based on an applied reference signal, comprising:

a charge pump system operatively coupled with an error detector and configured to produce a charge pump output; and

a voltage controlled oscillator operatively coupled with the charge pump system and configured to produce the output signal based on the charge pump output,

where the charge pump output includes a charge pump current that is scalable via selective operation of an inverse programmable current mirror in order to vary bandwidth response of the phase-locked loop.

44. The phase-locked loop of claim 43, where the inverse programmable current mirror is provided with a multistage configuration.

45. The phase-locked loop of claim 43, where the inverse programmable current mirror includes:

a reference system configured to receive a dynamic biasing signal; and

a mirror system operatively connected to the reference system and configured to output a scaled copy of the dynamic biasing signal, where the scaled copy of the dynamic biasing signal is scaled down by a mirror factor and applied to bias a charge pump within the charge pump system,

where the reference system includes a plurality of transistor groups, each transistor group being configured to alter the mirror factor via programmable variation of a dimensional parameter associated with the transistor group,

and where alterations to the mirror factor produced by one of the transistor groups are scaled relative to alterations produced by another of the transistor groups.

46. A phase-locked loop configured to produce an output signal based on an applied reference signal, comprising:

an error detector configured to produce an error signal for each cycle of the reference signal;

a charge pump operatively coupled to the error detector and configured to produce a charge pump output based on error signals generated at the error detector;

an oscillator operatively coupled with the charge pump and configured to produce the output signal based on the charge pump output; and

a gating system coupled between the error detector and charge pump, the gating system being configured to quantitatively reduce the charge pump output by gating the error signals generated by the error detector so that only a portion of the error signals are applied to the charge pump.